LISTING OF CLAIMS

Claim 1 (Original): A semiconductor integrated circuit comprising:

a function block arranged on a substrate;

a first buffering cell arranged adjacent to a first side of the function block;

a second buffering cell arranged adjacent to a second side adjacent to the first side of the function block; and

signal wiring passing over the function block obliquely relative to the first side and the second side, connecting the first buffering cell and the second buffering cell.

Claim 2 (Original): The semiconductor integrated circuit of claim 1, further comprising:

a first signal wiring extending in an X direction, which extends obliquely relative to the signal wiring; and

a second signal wiring extending in a Y direction, which is perpendicular to the first signal wiring and extends obliquely relative to the signal wiring.

Claim 3 (Original): The semiconductor integrated circuit of claim 2, wherein the signal wiring is arranged in a layer higher than the layer in which the first signal wiring and the second signal wiring are arranged.

Claim 4 (Original): The semiconductor integrated circuit of claim 2, wherein the signal wiring has an intersecting angle either 45 degrees and 135 degree relative to either of the first signal wiring and the second signal wiring.

Claim 5 (Original): The semiconductor integrated circuit of claim 1, wherein the signal wiring is a global signal wiring including one of a data bus and an address bus, arranged substantially in the entire area on the substrate.

Claim 6 (Original): The semiconductor integrated circuit of claim 1, wherein the first buffering cell and the second buffering cell are arranged outside of the function block.

Claim 7 (Withdrawn)

Claim 8 (Original): A semiconductor integrated circuit comprising:

a function block arranged on a substrate;

a plurality of signal wirings having a length shorter than a length of a side of the function block on the substrate;

a plurality of buffering cells electrically connected in series between each of the signal wirings; and

a signal wiring passing obliquely across the corner between a first side and a second side of the function block, which connects the buffering cells arranged adjacent to the first side and adjacent to the second side adjacent to the first side of the function block.

Claims 9-13 (Withdrawn)